WHAT IS CLAIMED IS:

1. A flat panel display comprising a luminescent device; and first and second transistors for driving the luminescent device, wherein the first and second transistors have different resistance values.

2. The flat panel display according to claim 1, wherein the first transistor is a driving transistor for driving the luminescent device, the second transistor is a switching transistor for switching on and off of the driving transistor, and the driving transistor has a higher resistance value than the switching transistor.

3. The flat panel display according to claim 1, wherein a transistor having a higher resistance value in the first and second transistors includes multiple gates, a semiconductor layer having high concentration source/drain regions, and an offset region formed on the semiconductor layer between the multiple gates.

4. The flat panel display according to claim 1, wherein a transistor having a higher resistance value in the first and second transistors includes a gate electrode, high concentration source/drain regions formed on both sides of the gate electrode, and an offset region formed between the gate electrode and the drain region.

5. The flat panel display according to claim 3 or claim 4, wherein the offset region is a high resistance region comprised of a low concentration impurity region on which low concentration impurities having the same conductivity type as the high concentration

source/drain regions are doped as a whole or partially doped, or a high resistance region comprised of an intrinsic region on which impurities are not doped.

6. The flat panel display according to claim 3 or claim 4, wherein the offset region is a high resistance region having a zigzag shape.

7. The flat panel display according to claim 1, wherein a transistor having a higher resistance value in the first and second transistors includes high concentration source/drain regions having different geometrical structure to have different resistance values, and a region connected to the luminescent device in the high concentration source/drain regions has a higher resistance value compared with the other region.

8. The flat panel display according to claim 1, wherein a transistor having a higher resistance value in the first and second transistors includes high concentration source/drain regions having different sizes to have different resistance values, and a region connected to the luminescent device in the high concentration source/drain regions has a smaller size compared with the other region.

9. The flat panel display according to claim 8, wherein the region connected to the luminescent device in the high concentration source/drain regions of the transistor has the same width and a longer length, or the same length and a narrower width compared with the other region.

10. A flat panel display comprising R, G and B unit pixels, wherein at least one unit pixel of the R, G and B unit pixels includes at least two or more transistors, each having source/drain regions, wherein at least drain region in the source/drain regions of at least one transistor in the transistors has a resistance value different from at least drain region of the other transistor.

11. The flat panel display according to claim 10, wherein drain regions of the at least one transistor and the other transistor have resistance values which are different from each other by doping concentration difference of the drain regions.

12. The flat panel display according to claim 11, wherein the drain region of the at least one transistor is a region which is the same conductivity type as the drain region of the other transistor, and on which low concentration impurities are doped as a whole or partially, or a region on which impurities are not doped.

13. The flat panel display according to claim 10, wherein drain regions of the at least one transistor and the other transistor have resistance values which are different from each other by shape difference of the drain regions.

14. The flat panel display according to claim 13, wherein the drain region of the at least one transistor is formed in a zigzag shape.

15. The flat panel display according to claim 13, wherein the drain region of the at least one transistor has the same width and a longer length, or the same length and a narrower width

compared with the drain region of the other transistor.

16. The flat panel display according to claim 11 or claim 13, wherein the drain region of the at least one transistor includes an offset region of high resistance.

17. A flat panel display comprising R, G and B unit pixels, wherein at least one unit pixel of the R, G and B unit pixels includes at least two or more transistors, wherein resistance value of a gate region of at least one transistor in the transistors is different from resistance value of a gate region of the other transistor.

18. The flat panel display according to claim 17, wherein the gate regions of the at least one transistor and the other transistor have resistance values which are different from each other by doping concentration difference of the gate regions.

19. The flat panel display according to claim 18, wherein the gate region of the at least one transistor is a region on which low concentration impurities are doped as a whole or partially, or a region on which impurities are not doped.

20. The flat panel display according to claim 17, wherein the gate regions of the at least one transistor and the other transistor have resistance values which are different from each other by shape difference of the gate regions.

21. The flat panel display according to claim 20, wherein the gate region of the at least

one transistor is formed in a zigzag shape.

22. The flat panel display according to claim 20, wherein the gate region of the at least one transistor has a longer length or narrower width compared with gate region of the other transistor.

23. The flat panel display according to claim 18 or claim 20, wherein the at least one transistor includes multiple gates, and an offset region of high resistance between the multiple gates.